SEMICONDUCTOR APPARATUS

BACKGROUND OF THE INVENTION

FIELD OF THE INVENTION

This invention relates to a semiconductor apparatus including a semiconductor device, used for ultra-high frequency signal processing of several GHz or more, or high-speed optical communication of several Gbps or more.

DESCRIPTION OF THE RELATED ART

The structure of a conventional semiconductor apparatus will now be briefly described.

The conventional semiconductor apparatus has a structure in which a semiconductor device is mounted on a dielectric board and is surrounded by a dielectric ring, with a metal cover mounted on the dielectric ring so as to cover the semiconductor device. Plural external electrodes for connecting with other external devices are arranged on the dielectric board. A thin metal wire is connected to the semiconductor device, and the thin metal wire is electrically connected with the external electrodes via a wiring arranged on the dielectric board.

On the back side of the dielectric board having the semiconductor device mounted thereon, a metal plate for radiation is bonded, and plural through holes are formed in the dielectric board so as to connect this metal plate with

the semiconductor device.

Literature 1: JP-A-5-129462

Literature 2: JP-A-7-50362

However, in the conventional semiconductor apparatus, the wiring connecting the semiconductor device with the external electrodes is formed by a conductor layer formed on the dielectric board and a single through hole, as disclosed in JP-A-7-50362. In this structure, since the conductor layer and the through hole are at right angles to each other, large parasitic capacitance is generated in the wiring. Therefore, there is a problem that input/output of a particularly high-frequency signal between the semiconductor apparatus and an external device is difficult.

SUMMARY OF THE INVENTION

In order to solve the foregoing problem, a semiconductor apparatus according to this invention includes: a semiconductor device; a first dielectric board surrounding the semiconductor device; a second dielectric board surrounding the semiconductor device and arranged on the first dielectric board; a metal cover arranged on the second dielectric board so as to cover the semiconductor device; plural external electrodes; a first through-hole wiring penetrating the first dielectric board and electrically connected with external electrodes; a second through-hole wiring penetrating the

second dielectric board and electrically connected with the semiconductor device; and an internal wiring inserted between the first dielectric board and the second dielectric board; the semiconductor device being connected with the external electrodes via the first through-hole wiring, the second through-hole wiring and the internal wiring; the first through-hole wiring and the second through-hole wiring being electrically connected with the internal wiring while being away from each other.

In this invention, the first through-hole wiring electrically connected with the external electrodes, the second through-hole wiring penetrating the second dielectric board and electrically connected with the semiconductor device, and the internal wiring inserted between the first dielectric board and the second dielectric board are provided. The semiconductor device is connected with the external electrodes via the first through-hole wiring, the second through-hole wiring and the internal wiring. The first through-hole wiring and the second through-hole wiring are electrically connected with the internal wiring while being away from each other. Therefore, the semiconductor device and the external electrodes are connected with each other by a zigzag wiring, that is, the nearly linear wiring, compared with a wiring bent at right angles in its halfway part. Thus, in this invention, since reduction in quantity of passed electric signal and

increase in quantity of reflected electric signal at a high frequency can be restrained, input/output of electric signals between the apparatus and an external device can be carried out efficiently.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a plan view showing semiconductor apparatuses of first, second and third embodiments.

Fig. 2 is a sectional view showing the semiconductor apparatus of the first embodiment.

Fig. 3 is a sectional view showing a modification of the semiconductor apparatus of the first embodiment.

Fig. 4 is a sectional view showing the semiconductor apparatus of the second embodiment.

Fig. 5 is a sectional view showing the semiconductor apparatus of the third embodiment.

Fig. 6 shows the quantity of passed electric signal with respect to frequency in the case a semiconductor device and external electrodes are connected with each other using one through hole and in the case the semiconductor device and the external electrodes are connected with each other using two through holes.

Fig. 7 shows the quantity of reflected electric signal with respect to frequency in the case a semiconductor device and external electrodes are connected with each other using

one through hole and in the case the semiconductor device and the external electrodes are connected with each other using two through holes.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

First Embodiment

Fig. 1 is a plan view showing semiconductor apparatuses of first, second and third embodiments of this invention. The embodiments of this invention are the same, when shown in a plan view. Therefore, the plan view is shared in the description these embodiments. In the plan view of Fig. 1, in order to show the internal structure of the semiconductor apparatus, a metal cover 15 is not shown. On the other hand, Fig. 2 is a sectional view showing the semiconductor apparatus of the first embodiment of this invention. Fig. 2 shows a cross section along a dotted line XY in Fig. 1. Fig. 3 is a sectional view showing a modification of the first embodiment of this invention. The first embodiment of this invention will now be described with reference to Figs. 1, 2 and 3.

In the semiconductor apparatus of this invention, a metal plate 11 having a semiconductor device 12 mounted thereon, and lead terminals 18 equivalent to external electrodes in the appended claims are arranged on the same virtual plane. The lead terminals 18 are for electrically connecting this semiconductor apparatus with another external device. Plural

lead terminals 18 are arranged around the metal plate 11. The metal plate 11 and the lead terminals 18 have substantially the same thickness.

A first dielectric board 13a is arranged, extending onto the metal plate 11 and the lead terminals 18 as a common base. A second dielectric board 13b is further superposed on the first dielectric board 13a. The first and second dielectric boards 13a and 13b has an aperture at their central parts, where the metal plate 11 is exposed. In the part where the metal plate 11 is exposed, the semiconductor device 12 is mounted. In other words, the first dielectric board 13a and the second dielectric board 13b are surrounding the semiconductor device 12.

On the second dielectric board 13b, a metal cover 15 is placed via a dielectric ring 14. That is, the metal cover 15 is arranged above the semiconductor device 12.

Therefore, this semiconductor apparatus has a structure in which the semiconductor device 12 is enclosed by the metal plate 11, the first dielectric board 13a, the second dielectric board 13b, the dielectric ring 14 and the metal cover 15.

In Fig. 1, the lead terminals 18 partly protrude from the first dielectric board 13a and the second dielectric board 13b. However, if the entire lead terminals 18 are arranged within the outer edges of the first dielectric board 13a or the second dielectric board 13b as shown in Fig. 3, the semiconductor apparatus itself can be miniaturized. Although

not shown, providing spherical or hemispherical bump electrodes as the lead terminals 18 has the same effect.

Meanwhile, an upper wiring 17a is formed on the second dielectric board 13b. An internal wiring 17b is formed in such a manner that it is inserted between the first dielectric board 13a and the second dielectric board 13b. Moreover, in the first dielectric board 13a and the second dielectric board 13b, a lower through-hole wiring 17c and an upper through-hole wiring 17d are formed, respectively. The lower through-hole wiring 17c and the upper through-hole wiring 17d are equivalent to a first through-hole wiring and a second through-hole wiring of claim 1, respectively. The lower through-hole wiring 17c and the upper through-hole wiring 17d are arranged away from each other, when they are shown in a plan view like Fig. 1 or when they are shown in a sectional view like Fig. 2 showing a cross section of a plane that overlaps the lower through-hole wiring 17c and the upper through-hole wiring 17d in the plan view.

Next, electric connection between the semiconductor device 12 and the lead terminals 18 in the apparatus will be described. The semiconductor device 12 and the upper wiring 17a are connected with each other via a thin metal wire 16. The upper wiring 17a and the internal wiring 17b are connected with each other via the upper through-hole wiring 17d. The internal wiring 17b and the lead terminals 18 are connected

with each other via the lower through-hole wiring 17c. As a result, the semiconductor device 12 and the lead terminals 18 can be electrically connected with each other in the following order: the semiconductor device 12, the thin metal wire 16, the upper wiring 17a, the upper through-hole wiring 17d, the internal wiring 17b, the lower through-hole wiring 17c, and the lead terminals 18. The upper through-hole wiring 17d is arranged more closely to the semiconductor device 12 than the lower through-hole wiring 17c is. The thin metal wire 16, the upper wiring 17a, the upper through-hole wiring 17d, the internal wiring 17b, the lower through-hole wiring 17c, and the lead terminals 18 have impedance of a constant value. Thus, the total impedance when the semiconductor device is viewed from the lead terminals is set at a specific value (for example, 50 Ω).

As described above, in the first embodiment of this invention, the first through-hole wiring electrically connected with the external electrodes, the second through-hole wiring penetrating the second dielectric board and electrically connected with the semiconductor device, and the internal wiring inserted between the first dielectric board and the second dielectric board are provided. The semiconductor device is connected with the external electrodes via the first through-hole wiring, the second through-hole wiring and the internal wiring. The first through-hole wiring

and the second through-hole wiring are electrically connected with the internal wiring while being away from each other. Particularly, the second through-hole wiring is arranged more closely to the semiconductor device than the first through-hole wiring is, and the semiconductor device and the external electrodes are thus electrically connected with each other. Since the first embodiment of this invention has such a structure, the semiconductor device and the external electrodes are connected with each other by a zigzag wiring. The zigzag wiring described in this case represents a shape of a line bent left and right many times. The effect of connecting the semiconductor device with the external electrodes in the zigzag form will be described hereinafter.

Fig. 6 shows the quantity of passed electric signal with respect to frequency in the case the semiconductor device and the external electrodes are connected with each other using one through hole and in the case the semiconductor device and the external electrodes are connected in a zigzag form using two through holes. Fig. 7 shows the quantity of reflected electric signal with respect to frequency in the case the semiconductor device and the external electrodes are connected with each other using one through hole and in the case the semiconductor device and the external electrodes are connected in a zigzag form using two through holes. In Figs. 6 and 7, a solid line represents the connection using one through hole

and a dotted line represents the connection using two through holes.

In general, as the frequency of an electric signal rises, the quantity of passed electric signal decreases and the quantity of reflected electric signal increases. Therefore, input/output of the electric signal between the semiconductor apparatus and an external device tends to be disturbed. However, as seen from Figs. 6 and 7, when two through holes are used for connection, reduction in quantity of passed electric signal and increase in quantity of reflected electric signal are not very large even when the frequency of the electric signal rises. The reason for this characteristic is that when the semiconductor device and the external electrodes are connected with each other using only one through hole, the wiring as a whole has a shape that is bent at right angles at its halfway part. The wiring of such a shape has large capacitance in itself and therefore causes a large change in impedance with respect to the frequency. Then, as an electric signal with a high frequency passes through the wiring, the quantity of passed electric signal decreases and the quantity of reflected electric signal increases, disturbing efficient input/output of the electric signal between the semiconductor apparatus and the external device. Therefore, it is desired that the semiconductor device and the external electrodes are connected with each other using a wiring of a nearly linear

shape.

In the first embodiment of this invention, the semiconductor device and the external electrodes are connected with each other using the zigzag wiring, that is, the wiring of a nearly linear shape, compared with the wiring bent at right angles only once at its halfway part. Therefore, in this invention, reduction in quantity of passed electric signal and increase in quantity of reflected electric signal at a high frequency can be restrained, enabling efficient input/output of electric signals between the apparatus and the external device.

Second Embodiment

Fig. 1 is a plan view showing the semiconductor apparatuses of the first, second and third embodiments of this invention. Fig. 4 is a sectional view showing the semiconductor apparatus of the second embodiment of this invention. Fig. 4 shows a cross section along the line XY in Fig. 1. The second embodiment of this invention will now be described with reference to Figs. 1 and 4.

The second embodiment of this invention differs from the first embodiment in that an upper metal layer 29a is formed on a second dielectric board 23b and under a dielectric ring 24. The upper metal layer 29a is formed together with an upper wiring 27a on the second dielectric board 23b, but is not electrically connected therewith. Moreover, in the second

embodiment, a part of lead terminals 28 is adapted for grounding. The upper metal layer 29a is electrically connected with the lead terminal 28 for grounding and can be supplied with the ground potential. This enables construction of a structure in which the upper metal layer 29a that can be supplied with the ground potential is inserted between an internal wiring 27b and a metal cover 25. The second embodiment of this invention has substantially the same structure as that of the first embodiment except for the above-described parts and therefore the remaining parts of the structure will not be described further in detail.

As described above, the second embodiment of this invention has substantially the same effect as that of the first embodiment. Moreover, since the metal layer connected with the external electrode for grounding is arranged between the internal wiring and the metal cover, the parasitic capacitance generated between the wiring and the metal cover can be reduced when surface mounting is carried out.

Third Embodiment

Fig. 1 is a plan view showing the semiconductor apparatuses of the first, second and third embodiments of this invention. Fig. 5 is a sectional view showing the semiconductor apparatus of the third embodiment of this invention. Fig. 5 shows a cross section along the line XY in Fig. 1. The third embodiment of this invention will now be

described with reference to Figs. 1 and 5.

The third embodiment of this invention differs from the second embodiment in that a lower metal layer 39b is arranged under a first dielectric board 33a. Also in the third embodiment, similar to the second embodiment, a part of lead terminals 38 is adapted for grounding. The lower metal layer 39b is electrically connected with the lead terminal 38 for grounding, similarly to an upper metal layer 39a, and can be supplied with the ground potential. This enables construction of a structure in which an internal wiring 37b is inserted between the upper metal layer 39a and the lower metal layer 39b, both of which can be supplied with the ground potential. The third embodiment of this invention has substantially the same structure as that of the second embodiment except for the above-described parts and therefore the remaining parts of the structure will not be described further in detail.

As described above, the third embodiment of this invention has substantially the same effect as that of the second embodiment. Moreover, since the metal layers connected with the top and bottom of the internal wiring are connected with the external electrode for grounding, the parasitic capacitance generated in the internal wiring can be further reduced than in the second embodiment.

In the third embodiment, the parasitic capacitance can be reduced even when the upper metal layer 39a is not provided,

though its effect is not so significant as in the second embodiment.